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(54) Liquid crystal display device.

(57) In an active matrix type liquid crystal display device which drives liquid crystal by applying voltage via a thin film transistor to each of transparent display electrodes (15) arranged in a matrix form, source buses (19) are each composed of a transparent conductive bus (19A) formed by a transparent conductive layer extending along each column of the display electrodes (15) and a metal bus (19B) formed by a high melting point metal layer overlapping and extending along the transparent conductive bus (19A). An insulating layer (23) is coated almost all over the surface of a base plate (11) on which the source buses (19) are disposed. The insulating layer has slot-like windows (19D) each extending along one side of each display electrode (15) so that the surface of the corresponding metal bus (19B) is partly exposed. A bus segment (19C) formed by a conductivity metal layer fills each slot-window (19D) to make direct contact with the metal bus (19B). With such a source bus structure in which the high conductivity metal layer and the transparent conductive layer are connected through the high melting

point metal layer, the resistance value of the source bus (19) is small and remains stable for a long time.

FIG. 5C

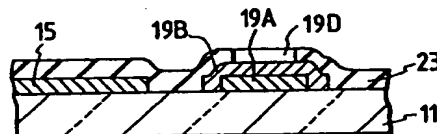
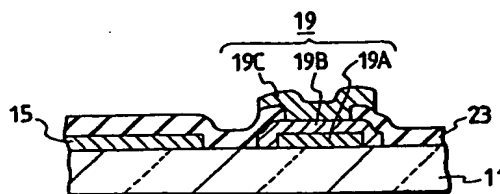


FIG. 5D



LIQUID CRYSTAL DISPLAY DEVICE

BACKGROUND OF THE INVENTION

The present invention relates to an active matrix liquid crystal display device which has a wide display area and provides a clear, highly precise display image accordingly.

A conventional liquid crystal display device of this kind has such a construction as shown in Fig. 1, wherein a pair of opposed transparent base plates 11 and 12 as of glass are separated by a spacer 13 interposed therebetween along their marginal portions and liquid crystal 14 is sealed in the space defined by the transparent base plates 11 and 12 therebetween.

The transparent base plate 11 has on its inside a plurality of display electrodes 15 and thin film transistors 16 formed as switching elements adjacent the display electrodes 15, drains of the thin film transistors 16 being connected to the display electrodes 15, respectively.

On the inside of the other transparent base plate 12 there is formed a transparent common electrode 17 opposite the display electrodes 15.

The display electrodes 15 are, for example, pixel electrodes. As depicted in Fig. 2, on the transparent base plate 11 square display electrodes 15 are closely arranged in a matrix form and gate and source buses 18 and 19 are formed close to the display electrodes 15 and extend along them in the row and column directions, respectively.

At the intersections of the gate and source buses 18 and 19 there are disposed the thin film transistors 16, which have their gates and sources connected to the gate and source buses 18 and 19 at their intersections and have their drains connected to the display electrodes 15.

Applying voltage across a selected one of each of the gate and source buses 18 and 19, only the associated thin film transistor 16 is turned ON and charges are stored in the display electrode 15 connected to its drain, applying voltage across only that portion of the liquid crystal 14 staying between the above-mentioned display electrode 15 and the common electrode 17. By this, only the above-said portion of the liquid crystal 14 corresponding to the display electrode 15 is rendered transparent or nontransparent to light, thus providing a selective display. This display can be erased by discharging the charges stored in the above-mentioned display electrode 15.

Figs. 3 and 4 show a prior art example of the thin film transistor 16. On the transparent base plate 11 the display electrode 15 and the source bus 19 are each formed by a transparent conductive film as of ITO and a semiconductor layer 22 as

of amorphous silicon is formed which bridges the gap between the display electrode 15 and the source bus 19 along their parallel-opposed marginal portions 15a and 19a which act as a drain electrode and a source electrode, respectively. The semiconductor layer 22 is covered with a gate insulating film 23 as of silicon nitride.

On the gate insulating film 23 there is formed a gate electrode 24 which overlaps the semiconductor layer 22 via the gate insulating film 23. The gate electrode 24 is connected at one end to the gate bus 18.

The drain and source electrodes 15a and 16a, the semiconductor layer 22, the gate insulating film 23, and the gate electrode 24 make up the thin film transistor 16. The gate electrode 24 and the gate bus 18 are simultaneously formed of a high conductivity metal such as aluminum (Al). Further, the drain and source electrodes 15a and 19a are covered with ohmic contact layers 25 and 26, which are formed by n⁺-type semiconductor layers, for example.

With the conventional liquid crystal display device of this kind, it is necessary, for providing a high-resolution display over a wide area, that the number of display electrodes be increased. In this instance, if the size of the display screen is fixed, the source buses 19 become narrower as the number of display electrodes increases, and if the pitch of the source buses 19 is fixed, they become longer with an increase in the number of display electrodes and hence with an increase in the size of the display screen. In either case, the resistance of each source bus 19 over the entire length thereof increases and the voltage drop thereacross also increases accordingly, so that uniform brightness cannot be obtained over the entire length of the source bus 19, resulting in a brightness gradient. That is, the farther away from the drive source, the lower the brightness.

The brightness gradient could be reduced by decreasing the resistance value of the source bus 19. One possible method therefor is to increase the cross-sectional area of the source bus 19 by increasing its width. However, an increase in the width of the source bus 19 will inevitably decrease the ratio of the sum of the areas of all the display electrodes 15 to the total area of the display screen (which ratio will hereinafter be referred to as the aperture ratio), leading to the degradation of the display quality.

Another method, which overcomes the above-mentioned defect, is to deposit a high conductivity metal layer on each source bus 19 over the entire length thereof to reduce its resistance value. If

aluminum which is used for the gate bus 18 is applied as well to the formation of the high conductivity metal layer, then it can be deposited on the source bus 19 simultaneously with the formation of the gate bus 18 without involving any particular step therefor. Consequently, the use of aluminum would be preferable in terms of the manufacturing process and cost.

Where the aluminum is deposited in direct contact with the ITO which forms the source bus 19, however, the subsequent annealing or similar heat treatment will allow oxygen in the ITO to combine with the aluminum in the interface therebetween, forming there an oxygen-aluminum combined layer. It has been found that the formation of the oxygen-aluminum combined layer increases the contact resistance between the ITO and aluminum layers, resulting in the resistance value of the source bus 19 becoming about the same as that of the ITO at the lowest.

Terminals of the gate buses 18 at one end are formed of ITO, partly because its contact resistance is stable and partly because they can be formed simultaneously with the formation of the display electrodes 15. Also in this instance, an oxygen-aluminum combined layer will be formed in the interface between the aluminum layer forming each gate bus 18 and the ITO layer forming the terminal as in the above case. The oxygen-aluminum combined layer increases the contact resistance between the aluminum and ITO layers, providing an equivalent circuit structure with a resistor interposed between the gate bus 18 and its terminal. Since the resistance values of these resistors are not uniform, the amplitude value of a drive signal scatters or differs with respective columns, introducing variations in the brightness of a display image.

Besides, the combination of the aluminum and the oxygen gradually proceeds in both of the gate buses 18 and the source buses 19 with the lapse of time, the conventional liquid crystal display device becomes less stable and hence cannot stand long use.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a liquid crystal display device which implements low-resistance bus structures which stably maintain their low-resistance properties for a long time.

In the liquid crystal display device of the present invention in which display electrodes and source buses are each formed by a transparent conductive layer, a metal bus of a high melting point metal is formed by deposition so that it

overlaps at least one marginal portion of the transparent conductive layer forming each source bus, and an insulating layer is formed on such metal buses almost all over a base plate. The insulating layer has a window which extends along one side of each display electrode to partly expose the top face of the metal bus, and the window is filled with a bus segment of a high conductivity metal layer which makes contact with the metal bus.

According to the present invention, the high conductivity metal layer is deposited on the high melting point metal layer so that the transparent conductive layer and the high conductivity metal layer do not make direct contact with each other. Consequently, no oxygen-metal combined layer forms in the interface between the transparent conductive layer and the high conductivity metal layer, and the source bus is stably held low in resistance by the high conductivity metal layer. Accordingly, no brightness gradient will develop, even if the source bus is not formed wide. Thus the liquid crystal display device of the present invention achieves high brightness and provides a highly precise display without reducing the aforementioned aperture ratio.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a sectional view of a liquid crystal display device for explaining the prior art;

Fig. 2 is a plan view schematically showing the arrangement of display electrodes and thin film transistors in the conventional liquid crystal display device;

Fig. 3 is a plan view showing a pattern of arrangement of electrodes, thin film transistors, source buses and gate buses in the conventional liquid crystal display device;

Fig. 4 is a sectional view of the thin film transistor taken on the line 4-4 in Fig. 3;

Figs. 5A through 5D are sectional views illustrating a sequence of steps involved in the formation of source buses in a first embodiment of the present invention;

Figs. 6A through 6D are sectional views illustrating a sequence of steps involved in the formation of gate bus terminals in the first embodiment of the present invention;

Fig. 7 is a plan view for explaining the plane structure of the liquid crystal display device of the present invention;

Figs. 8A through 8D are sectional views illustrating a sequence of steps involved in the formation of source buses in a second embodiment of the present invention;

Figs. 9A through 9D are sectional views illustrating a sequence of steps involved in the forma-

tion of gate bus terminals in the second embodiment of the present invention; and

Fig. 10 is a graph for explaining the effect of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring first to Figs. 5A through 5D, 6A through 6D and 7, the structure of the liquid crystal display device according to a first embodiment of the present invention will be described together with its manufacturing steps.

Figs. 5A through 5D are sectional views taken on the line 5-5 in Fig. 7 and Figs. 6A through 6D are sectional views taken on the line 6-6 in Fig. 7.

Fig. 7 shows the relative arrangement of the gate and source buses 18 and 19, the display electrode 15 and the thin film transistor 16.

The structural feature of the liquid crystal display device according to the first embodiment of the present invention resides in the source bus 19 depicted in Figs. 5A through 5D. The source bus 19 has a three-layer structure which comprises a transparent conductive bus 19A formed of ITO, a metal bus 19B formed by a high melting point metal layer on the transparent conductive bus 19A, and a bus segment 19C formed by a high conductivity metal layer on the metal bus 19B as shown in Fig. 5D.

Figs. 6A through 6D schematically illustrate the gate bus 18. As depicted in Fig. 6D, a gate bus terminal 18A is formed by a transparent conductive layer and a metal pad 18B is formed by a high melting point metal layer on the inner end portion of the gate bus terminal 18A. The gate bus 18 formed by a high conductivity metal layer is connected to the terminal 18A through a window 18C made in an insulating layer 23 overlying the metal pad 18B.

Next, a description will be given, with reference to Figs. 5A through 5D and 6A through 6D, of an example of the manufacturing process of the liquid crystal display device of the present invention.

The manufacture starts with the formation of the transparent conductive buses 19A of ITO on one side of the transparent base plate 11 at the position where to provide the source buses 19, as shown in Fig. 5A. In this step the display electrodes 15 and the gate bus terminals 18A are also formed of the ITO simultaneously with the formation of the transparent conductive buses 19A, as shown in Fig. 6A.

Incidentally, source bus terminals 19E (Fig. 7) are also formed by the ITO transparent conductive layer. That is, the transparent conductive buses 19A are formed to the edge of the transparent base plate 11 at one side thereof and their end portions

are used as the source bus terminals 19E.

The next step consists in forming the metal buses 19B by a high melting point metal layer which covers the transparent conductive buses 19A as shown in Fig. 5B. At the same time, the metal pads 18B are formed by the high melting point metal on the inner marginal portions of the gate bus terminals 18A as depicted in Fig. 6B. The high melting point metal usable for the metal buses 19B and the metal pads 18B is chromium (Cr), for instance.

In the next step the insulating layer 23, which serves also as a gate insulating film of each thin film transistor 16, is deposited all over the transparent base plate 11, and the insulating layer 23 is selectively removed by etching or the like, leaving required portions. At the same time, the insulating layer 23 is removed, as by etching, to form therein slot-like windows 19D to expose part of each metal bus 19B which will ultimately serve as the source bus 19 and the window 18C to expose part of each metal pad 18B of the high melting point metal layer overlying the gate bus terminal 18A as shown in Figs. 5C and 6C. Each window 19D extends along one side of corresponding display electrode 15 but terminates at the intersection of the gate and source buses 18 and 19 as depicted in Fig. 7.

The selective removal of the insulating layer 23 is followed by the formation of the segment buses 19C and the gate buses 18 by the same high conductivity metal layer. The gate buses 18 are connected to the metal pads 18B of the high melting point metal layer through the windows 18C made in the insulating layer 23, and the bus segments 19C are formed on each metal bus 19B, filling the windows 19D made in the insulating layer 23.

The high conductivity metal for the bus segments 19C and the gate buses 18 is aluminum as is the case with the gate electrodes. The high conductivity metal layer is deposited by evaporation or sputtering over the entire area of the surface of the insulating layer 23 and is selectively etched away, thereby providing such structures as shown in Figs. 5D and 6D. The bus segments 19C are not formed at the intersection of the source and gate buses 19 and 18 either.

Figs. 8A through 8D and 9A through 9D illustrate a second embodiment of the present invention.

In this embodiment the manufacture begins with simultaneous formation of the metal buses 19B and the metal pads 18B of a high melting point metal on the transparent base plate 11 at positions where the source buses 19 and the gate bus terminals 18A will ultimately be provided, respectively (Figs. 8A and 9A).

Next, the display electrodes 15, the gate bus

terminals 18A and the source bus terminals 19E (Fig. 7) are simultaneously formed by the same ITO transparent conductive layer. The gate bus terminals 18A and the source bus terminals 19E may also be formed of the high melting point metal, but since the electrical contact resistance of the high melting point metal layer as of chromium (Cr) is not stable, this embodiment utilizes the display electrode forming step to form the gate bus terminals 18A and the source bus terminals 19E by the transparent conductive layer.

In this embodiment two transparent conductive buses 19A are formed overlapping opposite marginal portions of each metal bus 19B of the high melting point metal deposited at the position where to form the source bus 19.

According to this method in which the transparent conductive bus 19A overlapping at least one marginal portion of each metal bus 19B, even if the metal bus 19B breaks off during formation thereof, the broken-off portion can be by-passed through the transparent conductive bus 19A. This improves the yield rate of product.

After the formation of the transparent conductive buses 19A and the gate bus terminals 18A, the insulating layer 23 is deposited substantially all over the base plate 11. The insulating layer 23 is selectively removed to form therein the windows 19D and 18C at predetermined positions on the metal buses 19B and the metal pads 18B in the same manner as described previously with regard to the first embodiment. After this, a high conductivity metal layer is deposited by evaporation or sputtering all over the surface of the insulating layer 23 and the high conductivity metal layer is selectively etched away to form the bus segments 19C for the source buses and the gate buses 18.

The bus segment 19C is not formed at the position where the source bus 19 intersects with the gate bus 18 as depicted in Fig. 7. One end portion of each gate bus 18 makes contact with the metal pad 18B through the window 18C.

As will be appreciated from the above, the structure of either embodiment of the present invention affords reduction of the resistance value of each source bus 19 by the deposition thereon of the plurality of bus segments 19C of the high conductivity metal. Thus the source bus 19 need not be widened for decreasing its resistance value, and consequently, the afore-mentioned aperture ratio is not reduced. Hence the liquid crystal display device of the present invention provides a high-brightness, high-precision display.

Moreover, each bus segment 19C is not in direct contact with the transparent conductive bus forming the source bus 19 but is connected thereto through the metal bus 19B of the high melting point metal layer. It is presumed from Fig. 10,

described later, that oxygen in the ITO forming the transparent conductive layer does not easily combine with the high melting point metal in the interface between the transparent conductive layer and the high melting point metal layer. Consequently, no change is caused in the contact resistances between the bus segments 19C by the high conductivity metal layer and the metal buses 19B by the high melting point metal layer and between the metal buses 19B and the transparent conductive buses 19A, so that the contact resistances can be stably held low for a long time.

Fig. 10 shows an example of the sum of measured values of the total resistance of the source bus, i.e. the resistance over the entire length of the source bus, and the contact resistance between the source bus and the terminal of the transparent conductive bus. In the case of the structure according to the present invention, when it was annealed at 180 and 280 °C, the sum of the contact resistance and the total resistance of the source bus was about 1 k Ω as indicated by circles in Fig. 10. In contrast thereto, in the case of the conventional structure composed of the aluminum and transparent conductive ITO layers, the above-mentioned sum of resistances scattered in the ranges of from 1 to 10 k Ω and from 5 to 100 k Ω as indicated by crosses when it was annealed at 180 and 280 °C, respectively.

Also in each gate bus 18, the contact resistance between the gate bus terminal 18A and the gate bus 18 will not increase, because the high conductivity metal layer forming the gate bus 18 is connected through the high melting point metal pad 18B to the gate bus terminal 18A formed by the transparent conductive layer. With such a structure, the amplitude of a drive signal to the thin film transistors 16 does not largely scatter for each row or column, and hence no appreciable variations occur in brightness, thus providing a stable display of image.

Although the above embodiments have been described to use chromium (Cr) for the high melting point metal layer, it is also employed nickel (Ni), molybdenum (Mo), tantalum (Ta), a nickel-chromium (Ni-Cr) alloy, or molybdenum-tantalum (Mo-Ta) alloy for the high melting point metal layer.

It will be apparent that many modifications and variations may be effected without departing from the scope of the novel concepts of the present invention.

Claims

1. An active matrix type liquid crystal display device which drives liquid crystal by applying voltage to display electrodes of transparent conductive

layer arranged in a matrix form on a transparent base plate, through thin film transistors disposed at intersections of source and gate buses, comprising: transparent conductive buses each formed by the same transparent conductive layer as those of said display electrodes and extending along each column of said display electrodes;
 metal buses each formed by a high melting point metal layer overlapping and extending along said transparent conductive bus, each of said source buses being composed of said transparent conductive bus and said metal bus;
 an insulating layer formed almost all over said base plate and having a slot-like window extending along one side of each of said display electrodes in the column direction and partly exposing therethrough the surface of said metal bus; and
 bus segments each formed by a high conductivity metal layer filling said slot-like window of said insulating layer to directly cover said exposed surface of said metal bus.

2. The liquid crystal display device of claim 1 wherein each said metal bus covers said transparent conductive bus substantially over the entire length thereof.

3. The liquid crystal display device of claim 2 which further includes gate bus terminals formed by the same transparent conductive layer as that of said transparent conductive buses and arranged side by side on one marginal portion of said base plate, and metal pads each formed on one of said gate bus terminals by the same high melting point metal layer as that of said metal buses, and in which said insulating layer further has a window formed therein at a position corresponding to each of said metal pads and said gate buses are each formed on said insulating layer by the same high conductivity metal layer as those of said bus segments, extend along each row of said display electrodes, and fill said window of said insulating layer to make direct contact with said metal pad on the corresponding gate bus terminal.

4. The liquid crystal display device of claim 1 wherein one marginal portion of each said transparent conductive bus overlaps one marginal portion of the corresponding metal bus over the entire length thereof.

5. The liquid crystal display device of claim 4 which further includes second transparent conductive buses formed by the same transparent conductive layer as that of first mentioned said transparent conductive buses, one marginal portion of each said second transparent conductive bus overlapping the other marginal portion of said corresponding metal bus, and in which said slot-like windows are made in said insulating layer to partly expose the surface of each said metal bus between the opposed edges of said two opposed transpar-

ent conductive buses.

6. The liquid crystal display device of claim 4 which further includes metal pads each corresponding to one of said gate buses and formed on another marginal portion of said base plate by the same high melting point metal layer as that of said metal buses, and gate bus terminals each formed by the same transparent conductive layer as that of said transparent conductive buses and overlapping one of said metal pads, and in which said insulating layer further has a window formed therein at a position corresponding to each of said metal pads and said gate buses are each formed on said insulating layer by the same high conductivity metal layer as those of said bus segments, extend along each row of said display electrodes, and fill said window of said insulating layer to make direct contact with the corresponding metal pad.

7. The liquid crystal display device of claim 3 or 6 wherein source bus terminals, formed by the same transparent conductive layers as that of said transparent conductive buses, are each connected to one end of said transparent conductive buses.

8. The liquid crystal display device of claim 1, 2, 3, 4, 5, or 6 wherein said high melting point metal layer is formed of chromium (Cr).

9. The liquid crystal display device of claim 1, 2, 3, 4, 5, or 6 wherein said high conductivity metal layer is formed of aluminum (Al).

10. The liquid crystal display device of claim 1, 2, 3, 4, 5, or 6 wherein said transparent conductive layer is formed of ITO.

FIG. 1
PRIOR ART

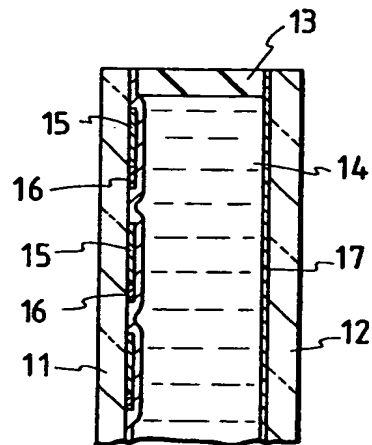


FIG. 2
PRIOR ART

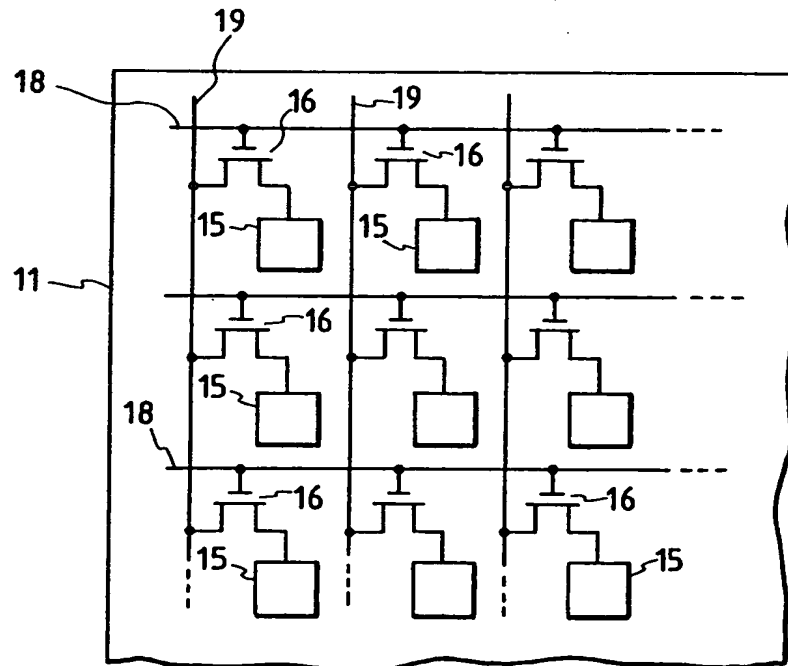


FIG. 3
PRIOR ART

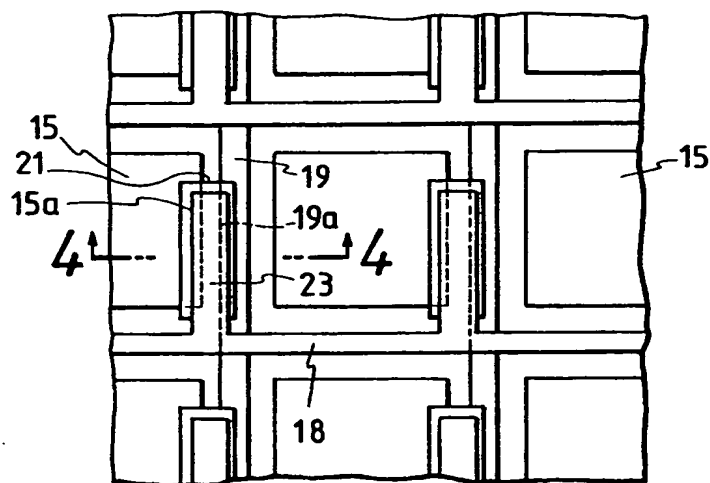


FIG. 4
PRIOR ART

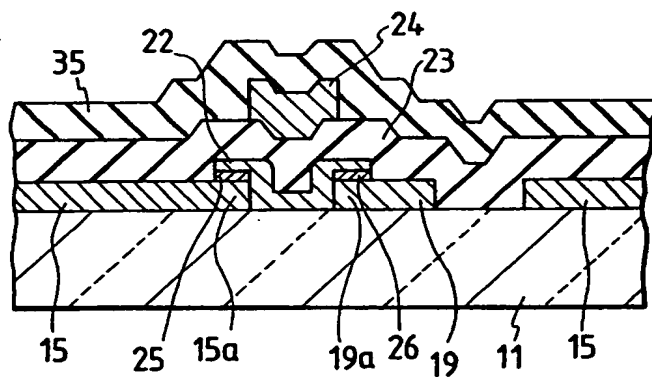


FIG. 5A

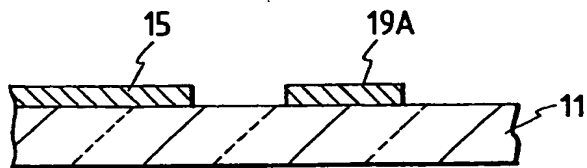


FIG. 5B

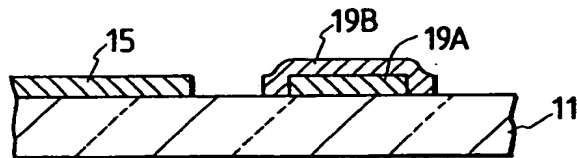


FIG. 5C

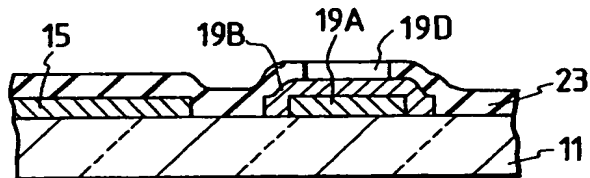


FIG. 5D

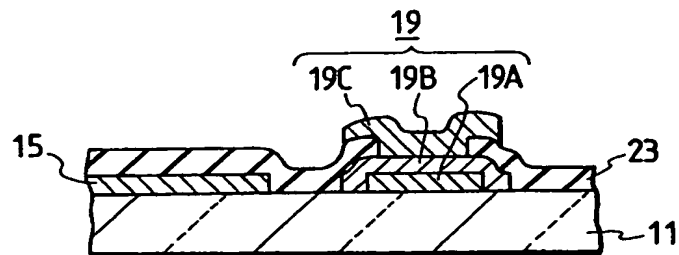


FIG. 6A

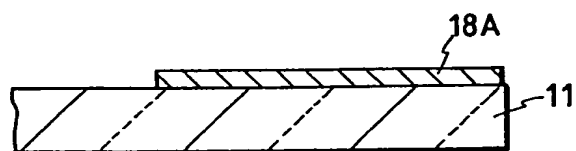


FIG. 6B

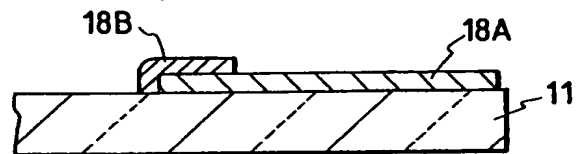


FIG. 6C

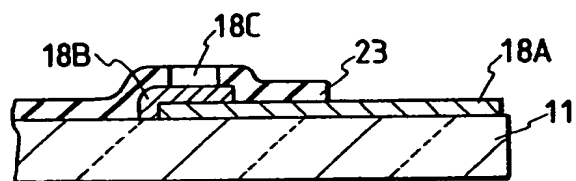


FIG. 6D

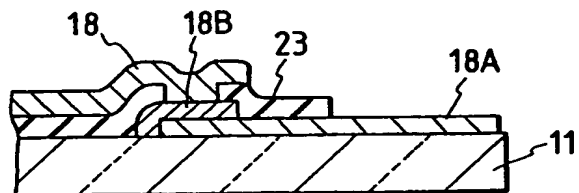


FIG. 7

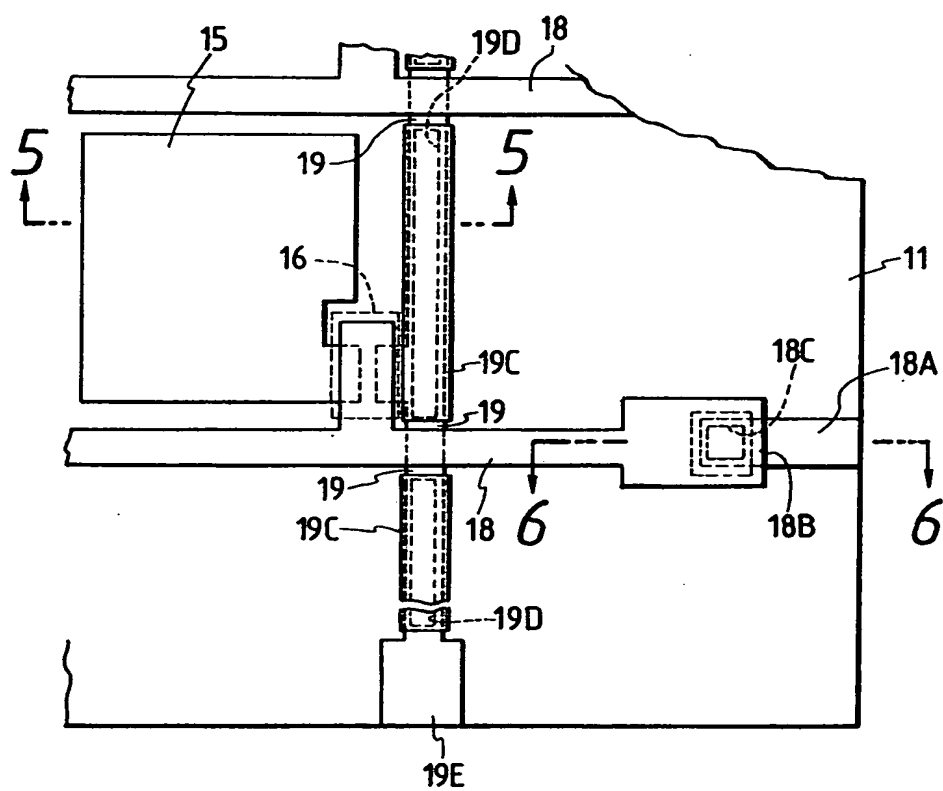


FIG. 8A

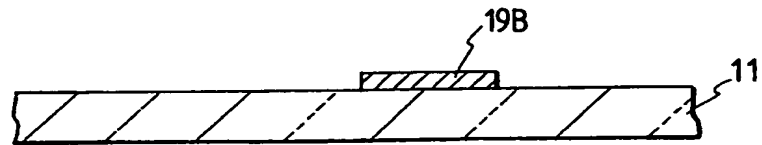


FIG. 8B

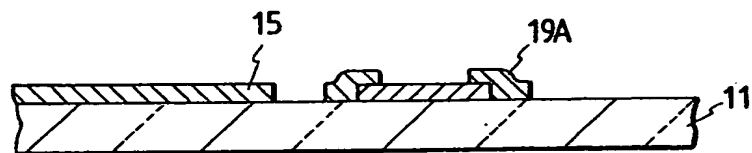


FIG. 8C

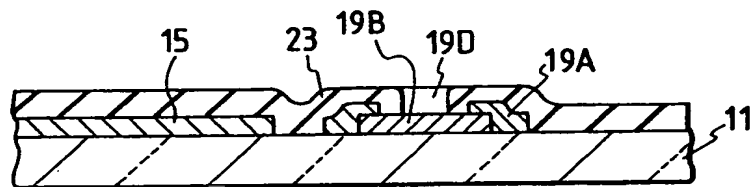
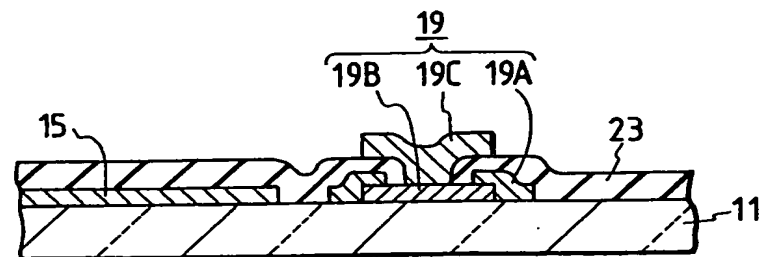


FIG. 8D



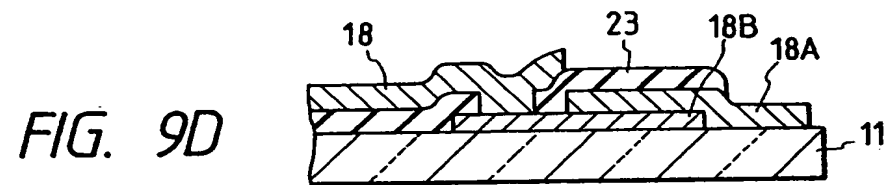
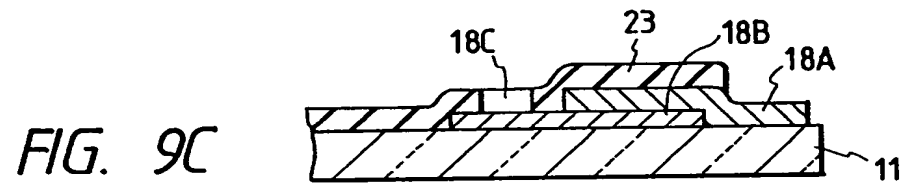
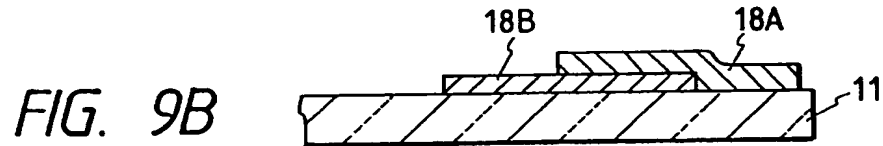
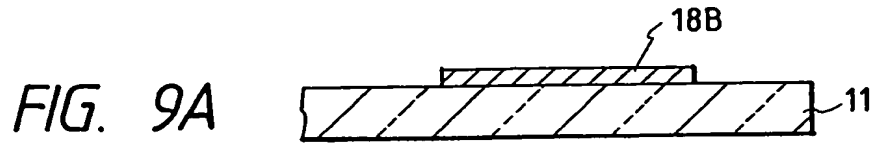


FIG. 10

